



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/649,078

08/27/2003

Frederick A. Perner

200205668-1

4664

22879

7590

05/01/2006

EXAMINER

LE, THONG QUOC

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

ART UNIT

PAPER NUMBER

2827

DATE MAILED: 05/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/649,078

Applicant(s)

PERNER ET AL.

Examiner

Thong Q. Le

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 February 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7,9-13,15,16,18-20 and 22-28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 6,7,9-13,15,16,18-20 and 22-24 is/are allowed.
- 6) ☒ Claim(s) 1 and 2 is/are rejected.
- 7) ☒ Claim(s) 3-5 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Amendment filed on 02/15/2006 has been entered.
2. Claims 1-7,9-13,15-16,18-20,22-28 are presented for examination.

Response to Arguments

3. Applicant's arguments with respect to claims 1-7,9-13,15-16,18-20,22-28 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Ikeda et al. (Pub. U.S. Patent No. 2002/0042515).

Regarding claim 1, Ikeda et al. disclose a method of increasing voltage available to a memory element ([0126], [0131]), comprising:

providing a current ([0126]) in a plurality of memory write lines (Figure 15, WWL, WL), wherein the write lines are magnetically coupled to at least one memory element ([0014], [0126], *example memory element R22 is selected*);

coupling a first and second plurality of transistors to either end of memory write line ([0126], *Figure 15, memory element R22, first transistor 712, second transistor T22*); and

altering the conduction state of individual transistors within the first and second plurality of transistors ([0131]).

Regarding claim 2, Ikeda et al. disclose wherein the amount of voltage available to the memory element is increasing ([0131], in column 10, *an increase of the voltage value*).

Allowable Subject Matter

6. Claims 3-5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3-5 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Ikeda et al. (Pub. U.S. Patent No. 2002/0041515), and others, does not teach the claimed invention having a method of increasing voltage available to a memory element including wherein the individual transistors within the first and second pluralities of transistors are coupled in parallel and are binary weighted as claim 3 disclosed, and wherein the amount of voltage available may be controlled by modifying the conduction state of the first and second plurality of transistors as claim 4 disclosed, and a coupling a power supplying to the first and second plurality of transistors wherein

Art Unit: 2827

the power supply has approximately constant voltage and providing a variable current as claim 5 disclosed.

Claims 6-7, 9-13, 15-16,18-19, 20,22-24, 25-28 are allowed.

Claims 6-7, 9-13, 15-16,18-19, 20,22-24, 25-28 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Ikeda et al. (Pub. U.S. Patent No. 2002/0041515), and others, does not teach the claimed invention having a memory comprising a plurality of transistors, wherein the individual transistors within the plurality of transistors are in parallel and have their conduction states modified independent of each other as claims 6-7, 9-13 disclosed, and wherein a threshold voltage for inverter is varied as the write signals is varied as claims 15-16,18-19 disclosed,, and a controlling means for controlling the conduction state of the providing means and the sinking means as claims 20,22-24 disclosed, and a computer system including an inverter coupled the first transistor, wherein the inverter controls the conduction state of the first transistor as claim 25-28 disclosed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2827

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thong Q. Le
Primary Examiner
Art Unit 2827

4/25/2006